

2 the control data processor is a general-purpose microprocessor that has an industry-  
 3 standard architecture,  
 4 whereby programs for the control data processor may be developed using standard tools for the  
 5 architecture.

R1.126 16. 1. The integrated circuit set forth in claim 14 wherein:  
 2 the streams of data include a serial stream and a parallel stream.

R1.126 17. 1. The integrated circuit set forth in claim 14 wherein the integrated circuit further comprises:  
 2 an aggregator that aggregates certain of the data stream processors so that the  
 3 aggregated data stream processors cooperate in processing a stream of data, the aggregator  
 4 including  
 5 configurable interconnections between the aggregated data stream processors;  
 6 a configurable operation coordinator that coordinates operation of the aggregated data  
 7 stream processors; and  
 8 a writeable configurator that specifies the configurable interconnections and the  
 9 configurable operation coordinator as required to aggregate the data stream processors.

R1.126 18. 1. The integrated circuit set forth in claim 14 wherein the integrated circuit further comprises:  
 2 a writeable configuration specifier for specifying a configuration of the data stream  
 3 inputs and/or outputs; and  
 4 configuration circuitry coupled between the plurality of I/O pins and the data stream  
 5 processor and responsive to the configuration specifier for configuring the inputs and/or  
 6 outputs as specified by the configuration specifier,  
 7 whereby the integrated circuit may be used with a plurality of transmission protocols.

R1.126 19. 1. The integrated circuit set forth in claim 14 wherein each data stream processor further  
 2 comprises:  
 3 a receive processor that operates under control of the control data processor to process  
 4 the data stream received from the data stream input and/or  
 5 a transmit processor that operates under control of the control data processor to process  
 6 the data stream for output to the data stream output.

21.126 20. 7. The integrated circuit set forth in claim <sup>19</sup>6 wherein each of the receive processor or the transmit processor further comprises:

3 a writeable instruction memory containing instructions; and

4 the receive processor or the transmit processor sequentially executes certain of the

5 instructions to process the data stream.

21.126 21. 8. The integrated circuit set forth in claim <sup>19</sup>6 wherein:

2 the receive processor and/or the transmit processor have a plurality of processing

3 components and are configurable to bypass one or more of the components in processing the

4 data streams.

21.126 22. 9. The integrated circuit set forth in any of claims <sup>14</sup>1 through 8 wherein the integrated circuit further comprises:

3 a context processor that responds to information received from a given data stream

4 processor that is processing a data stream to produce information about the given data stream's

5 context and provide the context information to the given data stream processor;

6 the given data stream processor using the context information to process the data stream.

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21.126 23. 10. The integrated circuit set forth in any one of claims <sup>14</sup>1 through <sup>21</sup>9 wherein:

2 a stream of data contains control data and payload;

3 a received stream of data is processed in a receiving data stream processor to extract

4 the control data and the payload and a transmitted stream of data is processed in a transmitting

5 data stream processor to add control data to the payload; and

6 the integrated circuit further comprises

7 a buffer manager coupled to the data stream processors that provides addresses of

8 buffers for storing payload and responds to a write operation with a buffer address to write

9 payload to the addressed buffer and to a read operation with a buffer address to read payload

10 from the addressed buffer; and

11 a queue manager coupled to the data stream processors that manages queues of

12 descriptors of payload, each descriptor including at least a buffer address, the queue manager

13 responding to an enqueue command by enqueueing a descriptor provided with the command to

14 a queue specified in the command and responding to a dequeue command by dequeueing a

15 descriptor from the queue specified in the command,